Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on a semiconductor substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein said first end of said via is connected to said first metal layer and said second end of said via terminates ~~prior to~~ at a termination point without reaching said second metal layer, said termination point be laterally spaced relative to the metal of the second metal layer.

2. (Original) The device as claimed in Claim 1, wherein said semiconducting device comprises an integrated circuit.

3. (Original) The device as claimed in Claim 1, wherein said insulating layer further comprises silicon oxide.

4. (Original) The device as claimed in Claim 2, wherein said integrated circuit further comprises complementary metal oxide-semiconductor, bipolar silicon, or group III-group V integrated circuits.

5. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on top of semiconductor

substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein said second end of said via is connected to said second metal layer and said first end of said via terminates ~~prior to~~ at a termination point without reaching said first metal layer, said termination point be laterally spaced relative to the metal of the first metal layer.

6. (Original) The device as claimed in Claim 5, wherein said semiconducting device comprises an integrated circuit.

7. (Original) The device as claimed in Claim 5, wherein said insulating layer further comprises silicon oxide.

8. (Original) The device as claimed in Claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor, bi-polar silicon, or group III-group V integrated circuits.

9. (Currently Amended) A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) disposing an insulating layer on top of semiconductor substrate;

(b) forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer; and

(c) forming a via defined by said insulating layer, said via having a first end and a second end,

wherein said first end of said via is connected to said first metal layer and said second end of said via terminates, ~~prior to~~ without reaching said second metal layer, at a point which is laterally spaced relative to the second metal layer.

10. (Withdrawn) The method as claimed in Claim 9, wherein said semiconducting device comprises integrated circuits.

11. (Withdrawn) The method as claimed in Claim 9, wherein said insulating layer further comprises silicon oxide.

12. (Withdrawn) The method as claimed in Claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor, bi-polar silicon, or group III-group V integrated circuits.

13. (Currently Amended) A method for preventing and/or thwarting reverse engineering, comprising steps of:

(a) disposing an insulating layer on top of semiconductor substrate;

(b) forming and patterning a first metal layer and a second metal layer so that said first metal layer and said second metal layer are separated by said insulating layer; and

(c) forming a via defined by said insulating layer, said via having a first end and a second end,
wherein said second end of said via is connected to said second metal layer and said first end of said via terminates, ~~prior to~~ without reaching said first metal layer, at a point which is laterally spaced relative to the first metal layer.

14. (Withdrawn) The device as claimed in Claim 13, wherein said semiconducting device comprises integrated circuits.

15. (Withdrawn) The device as claimed in Claim 13, wherein said insulating layer further comprises silicon oxide.

16. (Withdrawn) The device as claimed in Claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor, bi-polar silicon, or group III-group V integrated circuits.

17. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, including:

(a) an insulating layer disposed on a semiconductor substrate;

(b) a first metal layer and a second metal layer, said first metal layer and second metal layer being separated by said insulating layer; and

(c) a via defined by said insulating layer, said via having a first end and a second end,

wherein one end of said via is connected to one of said first metal layer and said second metal layer and wherein another end of said via terminates ~~prior to reaching~~ at a point which is laterally spaced from a least one of said first metal layer and said second metal layer.

18. (Currently Amended) A method for making a semiconductor device for preventing and/or thwarting reverse engineering thereof, comprising steps of:

(a) disposing an insulating layer on a semiconductor substrate;

(b) defining a first electrically conductive layer and a second electrically conductive layer so that said first electrically conductive layer and said second electrically

conductive layer are separated by said insulating layer; and

(c) defining a via in said insulating layer, said via having a first end and a second end, one of said first and second ends of the via contacting one of said first and second electrically conductive layers the other of said first and second ends of the via being laterally disposed relative to at least one of the first and second electrically conductive layers so that it contacts ~~contacting~~ neither one of said first and second electrically conductive layers whereby said via mimics a connecting via between said first and second electrically conductive layers without making an electrical connection between said first and second metal layers.

19. (Previously presented) A semiconductor device for preventing and/or thwarting reverse engineering thereof made according to the method of claim 18.

20. (Previously presented) The device as claimed in claim 1 wherein the first metal layer is an upper layer and the second metal layer is a lower layer relative to the insulating layer.

21. (Previously presented) The device as claimed in claim 5 wherein the second metal layer is an upper layer and the first metal layer is a lower layer relative to the insulating layer.